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10/563,040	07/17/2006	Jorg Berthold	1890-0274	6036

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MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
ROJAS, DANIEL E	
ART UNIT	**PAPER NUMBER**
4125	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,040	BERTHOLD ET AL.	
	Examiner	Art Unit	
	DANIEL ROJAS	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-39 and 42* is/are pending in the application.

4a) Of the above claim(s) *40-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-26,28-34, 37-39, and 42* is/are rejected.

7)☒ Claim(s) *27,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention 1, claims 23-39 and 42, in the reply filed on 11/23/2007 is acknowledged.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 29 and 30 are objected to because of the following informalities: misspelling. In claim 29, "to generate and inverted clock signal" should be "to generate an inverted clock signal." In claim 30, "switchs" should be "switches" and "the reference potential" should be "a reference potential." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The specification fails to teach a capacitor having a programmable capacitance. However, the specification does teach that "the capacitance C may be formed by a programmable capacitor network" (page 16, lines

35-36, specification) but fails to teach, both implicitly and explicitly, that the capacitance C may be a programmable capacitor.

6. "A circuit node arranged to charge to an operating voltage" is considered indefinite because it would be unclear to one of ordinary skill in the art how a node can be arranged to charge. Examiner notes that a node charging would violate Kirchoff's current law which teaches that the sum of the currents entering a node is equal to the sum of the currents leaving the node. For purposes of examination, examiner takes "a circuit node arranged to charge to an operating voltage" to mean "a circuit node arranged to charge a capacitor to an operating voltage."

7. Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant's drawings do not show four controllable switches being connected in series with each other between the circuit node and the reference potential node, as stated in the claim. However, for the purposes of examination, examiner will interpret this claim as "the first, second, third, and fourth controllable switches being connected in series with one another being a voltage supply and the reference potential node."

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 23-26, 28-34, 37-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klass (US Patent No. 5,197,355). Please refer to the figures below:

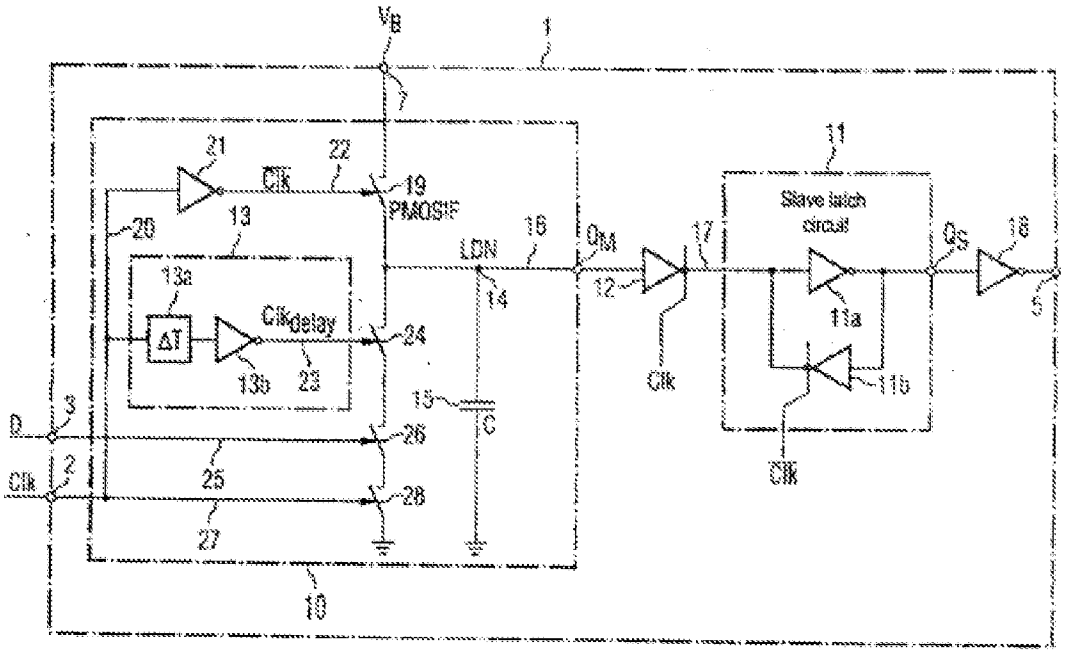

Figure 1: *Applicant's Invention*

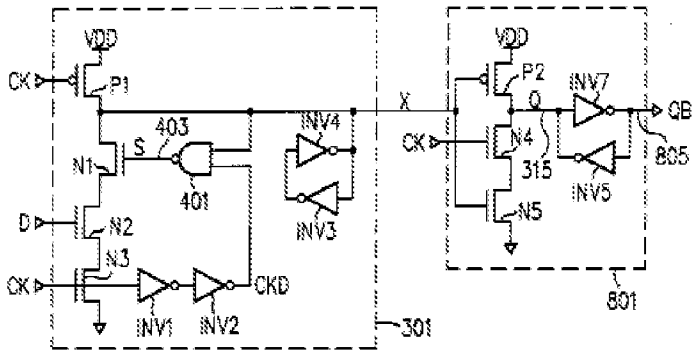

Figure 2: *Klass's invention (US Patent No. 5,917,355, Figure 8)*

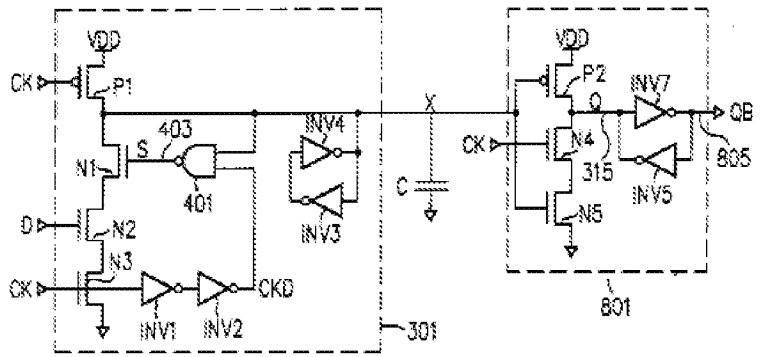

Figure 4: Combination Circuit

11. For claim 23, Klass's invention comprises a signal delay circuit (INV1 and INV2, Figure 2 above) configured to generate a delayed clock signal (CKD, Figure 2 above) corresponding to the clock signal (CK, Figure 2 above) delayed by a time delay (INV1 and INV2 in Figure 2 above form a buffer with a fixed time delay) but fails to teach the said circuit node and capacitor with a programmable capacitance. However, examiner takes official notice that it is notoriously old and well known that a capacitor connected to ground at an output to any circuit serves as a filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a capacitor directly connected between ground and node X of Klass's invention in order to filter

noise. Thus, the combination circuit of Klass's invention with the capacitor as described above (Figure 4) comprises a circuit node (X, Figure 4 above) arranged to charge a capacitor (C, Figure 4 above) in a charging phase in response to the clock signal being logically low (as explained below) and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed clock signal being logically high; and a capacitor with a programmable capacitance (see paragraph 4 of this action) coupling the circuit node (X, Figure 4 above) to a reference potential (ground). For Figure 4 above, when the clock signal is logically low, transistor P1 is on, allowing capacitor C to charge. The capacitor C discharges only when the clock signal (CK), input D, and the delayed clock signal (CKD) are all high.

12. For claim 24, the combination circuit of Figure 4 comprises a circuit node that is arranged to discharge a capacitor in the evaluation phase in response to the data signal being logically high and the circuit node is arranged to not discharge a capacitor in the evaluation phase in response to the data signal being logically low. As described above, the capacitor discharges when CK, CKD, and input D are high and charges when the signal CK is low. The charging of capacitor C does not depend on input D. Nonetheless, the capacitor C does not discharge when the data signal is low and CK is low.

13. For claim 25, the combination circuit of Figure 4 comprises a first isolating circuit (transistor N4, Figure 4 above) configured to be clocked by the clock signal and having an input connected to the circuit node (X, Figure 4 above).

14. For claim 26, the combination circuit comprises a slave latch circuit (INV7 and INV5) wherein the first isolating circuit has an output (drain of N4) connected to the slave latch circuit, the first isolating circuit configured to generate an output signal (Q) at the output, and the slave latch circuit is configured to buffer-store the output signal.

15. For claim 28, Figure 4 shows that the said signal delay circuit, the circuit node, and the capacitor are incorporated into a master latch circuit since the output X is inputted into the a second latch.

16. For claim 29, the combination circuit of Figure 4 teaches a first controllable switch that switches the operating voltage to the circuit node in response to the clock signal being logically low but fails to teach the inverter and first controllable switch driven by the inverted clock signal. However, examiner takes official notice that it is well known that a switch that is active low operates in the same manner as a switch that is active high which has an inverter connected to its control terminal. Therefore, it would have been obvious to one of ordinary skill in the art to substitute a PMOS transistor for the claimed first controllable switch driven by the inverted clock signal.

17. For claim 30, the combination circuit of Figure 4 comprises a master latch circuit which further includes a reference potential node (any node between ground and the source of transistor N3) configured to be coupled to the reference potential (ground); the master latch circuit further includes a second, third and fourth controllable switches, the first, second, third, and fourth controllable switches being connected in series with one another between a voltage supply (VDD) and the reference potential node.

18. For claim 31, the combination circuit of Figure 4 comprises a NAND gate within the master latch circuit which has a delayed clock signal and the output of the first controllable switch as inputs. Depending on the logic value of the output of the first controllable switch, the NAND gate will invert the delayed clock signal and send this signal to the gate of the second transistor (N1). Therefore, the master latch circuit is configured to generate a delayed inverted clock signal and to drive the second controllable switch with the delayed inverted clock signal.

19. For claim 32, in the combination circuit of Figure 4, the input signal D is connected to the gate of the third transistor (N2). Therefore, the third controllable switch (N2) is arranged to be driven by the data signal (D).

20. For claim 33, in the combination circuit of Figure 4, CK is connected to the gate of the fourth transistor (N3). Therefore, the fourth controllable switch (N3) is arranged to be driven by the clock signal.

21. For claim 34, in the combination circuit of Figure 4, the capacitor C is connected in parallel with N1, N2, and N3.

22. For claim 37, Figures 5 and 6 of Klass's patent show by inspection that the time delay is less than a time period of the clock cycle.

23. For claim 38, the references as applied above teach all of the claimed limitations.

24. For claim 39, by inspection of Figure 4, the master latch circuit only receives a single supply voltage (VDD).

25. For claim 42, the references as applied above teach all of the claimed limitations.

Allowable Subject Matter

26. Claims 27, 35, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. R./
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125